Remarks

The various parts of the Office Action (and other matters, if any) are discussed below under appropriate headings.

Request for Telephone Interview

Upon consideration of this reply by the Examiner, the undersigned respectively requests a telephone interview with the Examiner and the Examiner's Supervisor to discuss any outstanding issues in an effort to advance the application to allowance. Pursuant to MPEP § 713.01, an Applicant Initiated Interview Request Form is submitted herewith.

Claim Rejections - 35 USC § 112

Claims 1-10 and 20 were rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the enablement requirement. Claim 1, as amended, recites a semiconductor device, which includes, *inter alia*, a source and a drain **consisting essentially of** silicide. Paragraph 7 of the Office Action states that "figure 1 of the specification appears to show a source (20) and drain (22) which are completely made of silicide; there are no doped silicon regions which form the source or the drain." Paragraph 7 of the Office Action goes on to assert that "doped silicon source and drain regions *are necessary* for a MOSFET; they provide the charge carriers (holes or electrons) which create the current flow." (emphasis added).

In short, this rejection appears to rest upon a misunderstanding of the scope of "consisting essentially of" as well as a belief that the claimed semiconductor device requires **doped** silicon source and drain regions.

With regard to the language "consisting essentially of", the Examiner's attention is directed to MPEP 2111.03, which states, "the transitional phrase 'consisting essentially of' limits the scope of a claim to the specified materials or steps 'and those that do not materially affect the basic and novel characteristic(s)' of the claimed invention". *In re Herz*, 537 F.2d 549, 551-52, 190 USPQ 461, 463 (CCPA 1976) (emphasis in original).

Second, the Examiner's statement regarding the necessity of doped silicon source and drain regions is unsupported by any evidence in or citation to the record. A FET-type device is characterized by control of majority carriers across a channel due to

an electric field established by the gate. Although doped source and drain regions are found in conventional FET-type devices, they are not required for the claimed invention.

In making this statement, the Examiner appears to be relying on his own personal knowledge and/or that knowledge that is generally available to one of ordinary skill in the art. In such a circumstance, applicant is to required to seasonably challenge statements by the Examiner that are not supported on the record, and failure to do so will be construed as an admission by the applicant that the statement is true. MPEP 2144.03. Therefore, in accordance with this duty, the Examiner is requested to cite some evidence that supports the Examiner's assertions. If the Examiner is unable to provide such evidence by way of a reference, and is relying on facts within his own personal knowledge, applicant is hereby requests that such facts be set forth in an affidavit from the Examiner pursuant to 37 C.F.R. §1.104(d)(2).

With respect to enablement under 35 U.S.C. § 112, MPEP 2164.04 instructs that "[a] specification disclosure which contains a teaching of the manner and process of making and using an invention in terms which correspond in scope to those used in describing and defining the subject matter sought to be patented must be taken as being in compliance with the enablement requirement of 35 U.S.C. 112, first paragraph, unless there is a reason to doubt the objective truth of the statements contained therein which must be relied on for enabling support".

In this regard, the Examiner's attention is directed to Page 3, line 30 of the application, which states that the source 20 and the drain 22 can be formed from a metal or metal-containing compound. In one embodiment of the invention, the source 20 and the drain 22 are formed by siliciding the layer of semiconductor material 18. The application goes on to state that a metal or metal containing source 20 and drain 22 provide for low parasitic resistance and form a Schottky junction between the source/drain 20/22 and the layer of semiconductor material 18 including the body region 24. Schottky junctions have a nonlinear rectifying characteristic such that majority carriers are predominant. For at least these reasons, claims 1-10 and 20 are compliant with the enablement requirement of 35 U.S.C. 112, first paragraph. Therefore, the rejection should be withdrawn.

Claim Rejections - 35 USC § 102 and § 103

Claim 1, as amended, recites a semiconductor device, which includes a source and a drain, where the source and the drain consist essentially of silicide, and a gate dielectric made from a material having a relative permittivity of greater than about 10.

As discussed above, with regard to the language "consisting essentially of", the Examiner's attention is directed to MPEP 2111.03, which states, "the transitional phrase 'consisting essentially of' limits the scope of a claim to the specified materials or steps' and those that do not materially affect the basic and novel characteristic(s)' of the claimed invention." *In re Herz*, 537 F.2d 549, 551-52, 190 USPQ 461, 463 (CCPA1976) (emphasis in original).

Wilting fails to disclose or fairly suggest a semiconductor device, which includes a gate dielectric made from a material having a relative permittivity of great than 10. Paragraph 10 of the Office Action states that, "there is a gate dielectric (4A, 4B), made of silicon oxide (4A) and silicon nitride (4B), which separates the gate electrode (16A) and the body."

Neither silicon oxide nor silicon nitride, standing alone as a single layer or formed together as stacked layers, constitute a gate dielectric made from a material having a relative permittivity of greater than 10. The Office Action's reliance on Lee for a showing that silicon oxide and silicon nitride (as used and disclosed by Wilting) are high-K materials is improper. First, at col. 5, lines 30-31, Lee does not discuss silicon oxide or silicon nitride. Rather, Lee discusses a "NO (Nitride-Oxide)" layer, which is not a conventional chemical expression, and, at best, can be interpreted as silicon oxynitride, which has a K of about 4-8.

Paragraph 2 of the Office Action asserts that a silicon oxynitride layer having a relative permittivity of about 4-8 anticipates a gate dielectric made from a material having a relative permittivity of greater than about 10. MPEP 2131.03 is instructive on anticipation of ranges. In short, the rejection is improper because the cited range of about 4-8 fails to touch, overlap or be within the claimed range of greater than 10.

In addition, Wilting fails to disclose or fairly suggest a semiconductor device, which includes a source and a drain consisting essentially of silicide. In fact, Paragraph 10 of the Office Action acknowledges that Wilting fails to disclose a source and a drain consisting essentially of silicide by pointing out that Wilting discloses source (41) and drain (42) regions having silicide zones (31, 32).

None of the cited references, including Grant, Venkatesan and Raajimakers, taken alone or in combination, disclose or fairly suggest the claimed invention. With regard to the rejection of claim 1 as being obvious over Grant in view of Wilting, it is respectively submitted that the Office Action fails to establish a *prima facie* case of obviousness.

Under 35 U.S.C. § 103(a), "[t]o establish a *prima facie* case of obviousness three basic criteria must be met. First, there must be some suggestion or motivation either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations."

First, Wilting fails to disclose or fairly suggest a semiconductor device, which includes a source and a drain consisting essentially of silicide. Wilting illustrates silicide drain zones (31, 32) within p-type drain zones (41, 42) (designated by dashed lines in Figs. 14-16), rather than source and drain regions consisting essentially of silicide. In addition, Grant makes no mention of silicide source and drain regions. In addition to failing to teach or suggest all the claim limitations, neither Wilting or Grant include sufficient suggestion or motivation to modify the references or combine the reference teachings.

Paragraph 4 of the Office Action discusses standards related to product by process claims. It is noted that the present application includes device claims having structural limitations. The present application does not include product by process claims.

For at least these reasons, it is respectively submitted that claim 1 and claims 2-10 dependent therefrom distinguish patentably over the references of record. Accordingly, the rejections should be withdrawn.

Claim 20, as amended, recites a semiconductor device including a source and a drain consisting essentially of silicide and a semiconductor body disposed between the source and the drain, wherein a source/body junction is defined by silicide material of the source and semiconductor material of the body and a drain/body junction is defined by silicide material of the drain and the semiconductor of the body.

None of the cited references, taken alone or in combination, disclose or fairly suggest source/body and drain/body junctions defined by silicide material of the source/drain and semiconductor material of the body. In addition, none of the cited references, taken alone or in combination, disclose or fairly suggest a source and a drain consisting essentially of silicide.

In this regard, it is respectively submitted that what is alleged in Paragraphs 14 and 21 of the Office Action is simply inaccurate. In particular, both of Paragraphs 14

and 21 of the Office Action point to figure 16 of Wilting for the teaching of source/body and drain/body junctions defined by silicide material of the source/drain and semiconductor material of the body. Figure 16 of Wilting, along with the associated description at col. 7, shows silicide source zone (31) within implanted p-type source zone (41) (shown by dashed line) and silicide drain zone (32) within implanted p-type drain zone (42) (shown by dashed line). As such, the source/body junction of the device disclosed in Wilting is defined by a p-type semiconductor material of source zone (41) as the semiconductor material of the body. Similarly, the drain/body junction of the Wilting device is defined by the p-type semiconductor material of drain zone (42) and the semiconductor material of the body. Grant, along with the other cited references, fail to cure the deficiencies of Wilting.

For at least these reasons, it is respectively submitted that claim 20 distinguishes patentably over the references of record. Accordingly, the rejections should be withdrawn.

Conclusion

In view of the foregoing, request is made for timely issuance of a notice of allowance.

Respectfully submitted,

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CERTIFICATE OF MAILING (37 CFR 1.8a)

I hereby certify that this paper (along with any paper or thing referred to as being attached or enclosed) is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: MS Non-Fee Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Date: 12/3/03

Jason A. Worgull

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